APPLICATION NOTE

Monitor ICs FAQs

AN96129

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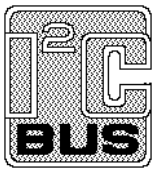
Abstract

In this application note the answers for customers FAQs (frequently asked questions) are provided for our monitor ICs' applications (such as for TDA4851/4852/4855/4858/4866/4885/8351) and related effects.



Purchase of Philips I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conforms to the I^2C specifications defined by Philips.

APPLICATION NOTE

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Summary

This application note is meant to answer 25 FAQs (frequently asked questions) for our monitor ICs‘ applications (such as for TDA4851/4852/4855/4858/4866/4885/8351) and some related effects. Hopefully this note can be an internal reference for new colleagues to provide proper solutions for customers’ similar problems in the future.

CONTENTS

1. INTRODUCTION

During this year we found some application questions or related issues were frequently inquired by customers. Now we collect some information from the emails (written by a.o. PS-SLE, Hamburg CIC) and related application notes to provide the answers and application hints for our monitor deflection ICs (TDA4851/4852/4855/4858/4866/8351) and video pre-amp (TDA4885). We hope this note can be an internal reference and help you to solve customers‘ problems.

To be easier to use this note you can check the issues list at page 7 first to find all the issues (questions) and related devices and the solution for each issue is described at the mentioned pages.

2. ISSUES

3. SOLUTIONS

3.1. Trapezium correction

The trapezium correction circuit for TDA4851/52 is depicted in figure 1.

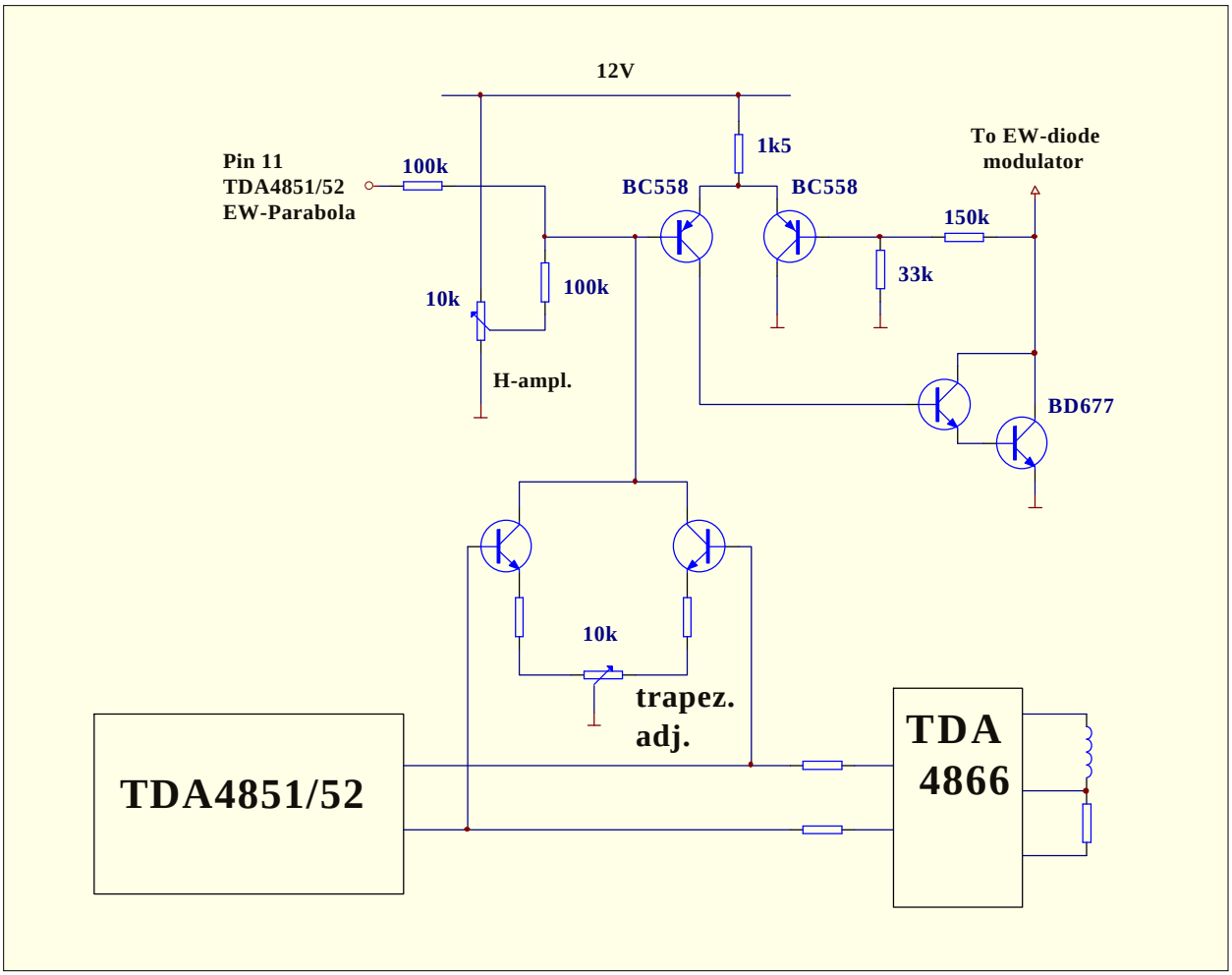

figure 1

3.2. Phase bending

1) With unsymmetrical EW-parabola
In this case the delay time of deflection transistor changes a little from bottom to top of the screen. The capacitor at TDA4855/58 pin 31 should be reduced to decrease the PLL2 time constant.

2) With parallelogram correction
If the capacitor at TDA4855/58 pin 30 is too high this can create top bending if parallelogram correction is active in plus/minus position. Therefore we recommend to keep this capacitor not higher than 22 nF.

3.3. H-autosync range

The H-autosync range for TDA4855/58 is about 30 to 100 KHz. If we want to increase this range, for instance from 30 to 110 KHz, please refer to following application diagram figure 2. (the capacitors' values are roughly, transistor T is switched off when H-frequency over 90 kHz). With the two capacitors in parallel make a horizontal range from 30 to 90 KHz. With only one capacitor make a range up to 110 KHz.

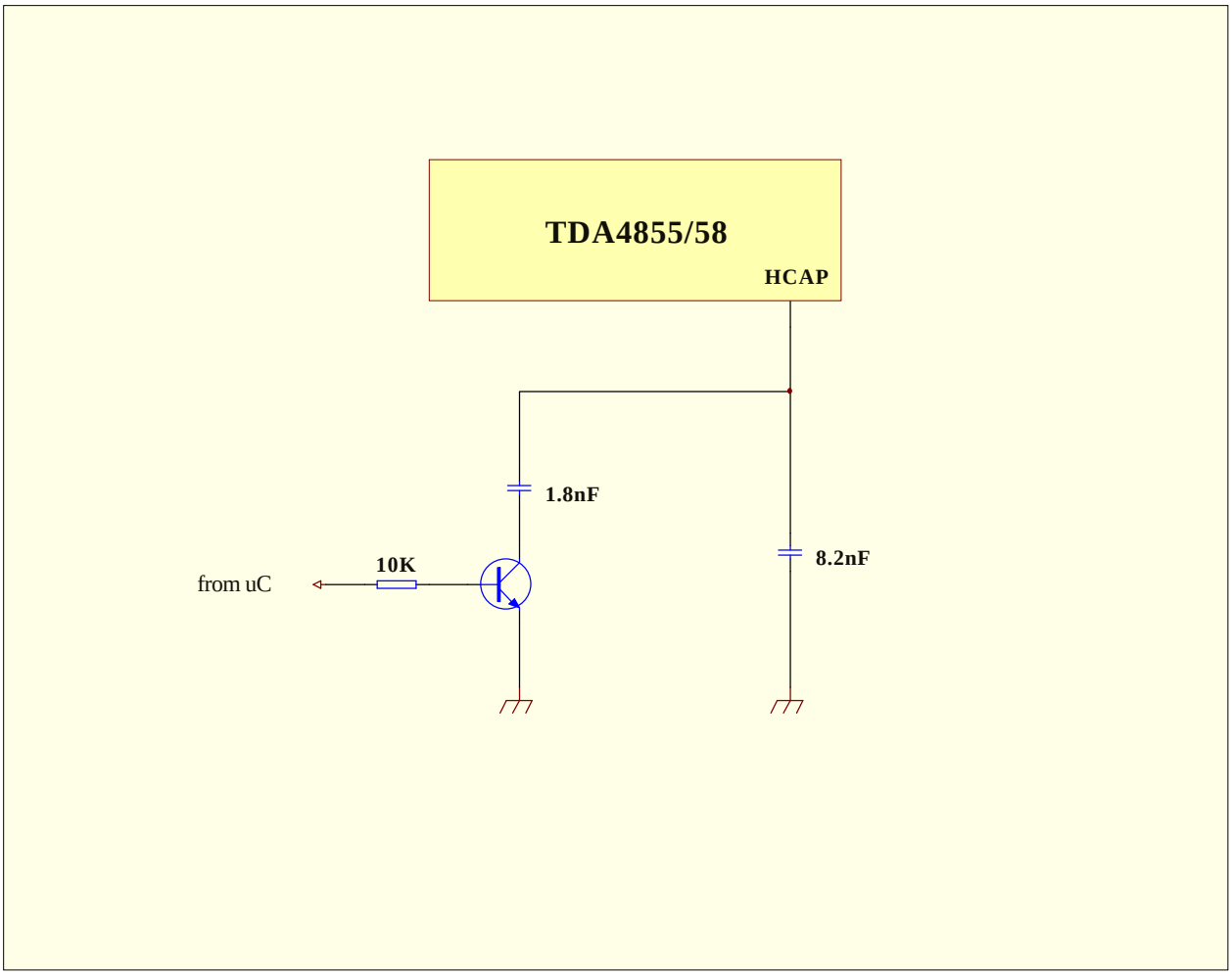

figure 2

3.4. H-pos range

An additional H-shift can be made with the PLL2 loop of TDA4855/58. This can be done with a resistor(about 1.2 M Ohm) from pin 31 to ground.

3.5. H-output

There are two possible causes as follows to damage the H-output transistor during mode changes.

1) Incorrect setting of the s-capacitors. The s-correction frequency is about half of the horizontal frequency, so if horizontal frequency is 60 KHz then the s-correction frequency is 30 KHz. When we switch the horizontal frequency from high to low, for instance from 60 to 31 KHz, then the deflection IC's oscillator is tracking very rapidly. In this case if the s-capacitors do not follow fast enough then the horizontal frequency is 31 KHz and s-correction frequency is still 30 KHz. Now there are two resonant systems at about the same frequency. This will cause an unwanted resonance rise and can overstress the H-output transistor.
2) Too slow decline of the B+ voltage. The B+ voltage should be tracking (linear) with horizontal frequency. At mode change deflection IC switches very fast to the low frequency. If the B+ voltage can not follow fast enough (in fact the voltage is too high for this new frequency) then the transistor will be overstressed.

3.6. Vertical s-correction

Additional vertical s-correction can be done with circuit depicted in figure 3. Pin 20 (EWTRP) of TDA4855/58 is used with double function. Current of pin 20 determines trapezium correction and the superimposed parabola voltage at pin 20 should not bring additional current.

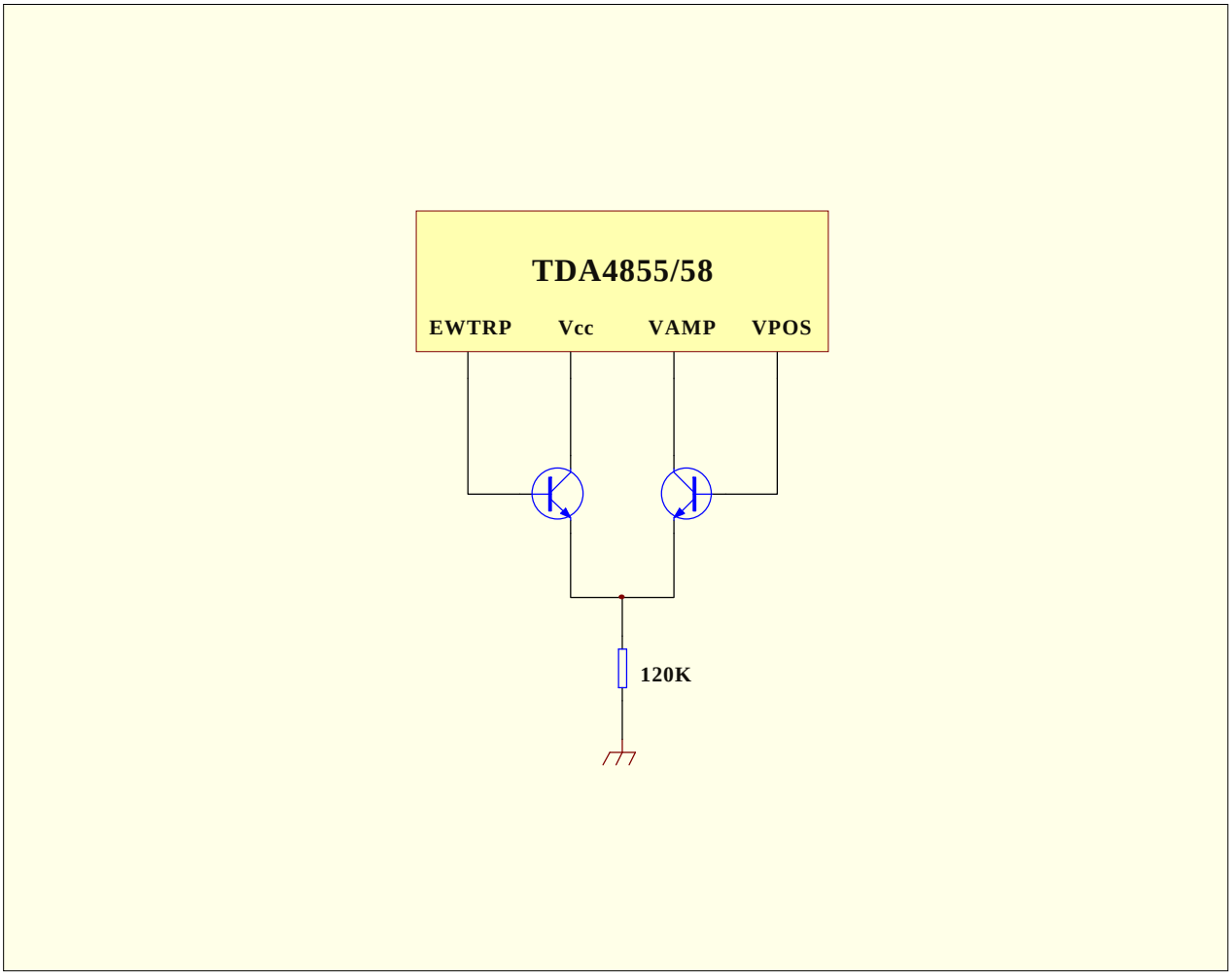

figure 3

3.7. Vertical linearity

The poor vertical linearity might be caused by a capacitor at TDA4855/58 pin 24(VCAP). The material of the VCAP capacitor is critical for good vertical linearity. If an additional vertical linearity correction is needed then please see Application Note AN95087 page 50 figure 53 for the application circuit.

3.8. V-size drift

There is a tendency for TDA4866 that V-size decreases with increasing temperature. A compensation is possible with the resistor at TDA4866 pin 4 or pin 9. For instance we can connect a resistor with negative Temperature Coefficient in parallel to Rm (please refer to TDA4866 data sheet Fig 4 application diagram for the position of Rm).

3.9. Retrace lines

Some general advices are as follows for TDA4866 when seeing visible lines at the start of vertical scan.

1) Check that the total resistor value in parallel with the vertical deflection coil is between 100 to 150 Ohm (130 Ohm nominal) including any resistor on the CRT/coil combination. This will provide fast settling after flyback without overshoot.

   On the TDA4866 data sheet, the resistor value mentioned for Rp is 390 Ohm (please see TDA4866 data sheet Fig 4 application diagram). However, this is only true when Philips CRT is used, which have an integrated symmetry potentiometer of 180 Ohm across the vertical deflection coil. So the total resistor value is approximately 130 Ohm.

2) Check the V-blanking concept of the customer. Basically there are two possibilities:

   a) Blanking pulse of the deflection ICs TDA485x is used (bottom part of sandcastle is extracted by a RC+transistor network and fed to grid 1). No lines will be visible if the total flyback + settling time is shorter than this blanking pulse.

   b) Blanking (=guard) pulse of the TDA4866 is used for blanking on grid 1. Many customers use this method. Since the guard pulse of our IC's covers only the actual flyback time but does not include the settling time, some lines will be visible in the top of the picture. This situation can be improved by extending the trailing edge of the guard pulse, for instance by means of a D-C-R network.

   Another problem is that the vertical scan starts in VGA mode after 575 us typically and in other mode after 300 us typically. A blanking procedure like a) would always avoid problem. However if customer uses the guard output of TDA4866 for V-blanking. This signal has to be delayed because the time is too short and does not cover the settling time of the deflection current. Besides, this method is not flexible with mode change. In this case the customer can use the uC to bring in the necessary flexibility. That is so far ok but the uC has to identify the VGA-mode (Fh<32 KHz) very properly and has to produce a vertical blanking pulse of 650 us or 360 us respectively.

3.10. V-autosync range

The vertical autosync range of TDA4855/58 can be extended via an application circuit as given in Application Note AN95087 page 35 figure29. For normal situation, like from 50 to 100 Hz, the transistor should be on. If the range should be extended to the higher frequency (above 100 Hz), the transistor should be switched off. For this purpose a signal coming from the uC can be used.

3.11. Pairing effect

A “pairing effect” (caused by overlap scanning) was found in the picture when displaying IBM 8514 interlaced mode. This will make the picture (the characters) unclear especially from the center to the bottom part of the picture.

From the theory we should not have problem with interlaced mode in case both half pictures contain the same figures of horizontal lines. There will be problem if an interlaced mode with 408 total lines in one half picture and 409 total lines in the other half picture then we will have a disturbance at the bottom of the screen and the pairing effect happened. To solve this we can increase the VAGC capacitor value at TDA4855/58 pin 22. In this case the lockin time will be increased but it should not be important.

3.12. Connection with defl. controller

Normally the vertical booster TDA4866 is used in combination with deflection controller TDA485x. In case another vertical booster TDA8351 is used i.s.o TDA4866 to connect to TDA485x, a resistor should be added between TDA8351 pin 1 and 2 since TDA8351 is voltage input type. Also pin 6 and 7 should be exchanged compared to TDA4866.

3.13. Sub-contrast

If customers want to have the sub-contrast setting with TDA4885, in case they do not use the gain modulation inputs meant for brightness uniformity, then these pins can be used very well for the sub-contrast. Just tie the three pins together and connect them to a sub-contrast potentiometer (or a free DAC of the uC). The DC control range must be from <1V to >3V.

If gain modulation pins are already used, the sub-contrast setting can be done by software only. Allocate a maximum value byte for factory alignment of sub-contrast and separate byte for user control. The available user contrast control range is then limited by software.

3.14. Smearing

For the smearing so far we have only experience with DC coupled video amplifier CR1296 like demo board. This board has a long term smearing of about 500 ns coming from video amp. The TDA4885 contributes a short term smearing of about 100 ns. We suggest to bring in an additional R/C-network in parallel to the speed up R/C-network. These additional components can be optimised to compensate the smearing. Values of 1K ohms and 220 pF give a good compensation for the board.

3.15. Beam current limiting

The beam current limiting(BCL) pin of TDA4885 is a full copy from the same pin that you will find on all our TV IC's. So the application can be copied to. Here is a summary. The footpoint of the EHT winding of the FBT is connected with a resistor to +8V or +12V and decoupled by a filter capacitor to ground. Furthermore it is connected to the BCL input (LIM) of the TDA4885. When the (averaged) beam current exceeds the limit of the CRT, the voltage on the footpoint will fall below 4.5V. Any further increase in beam current is then counteracted because it pulls pin LIM low and consequently the contrast (and beam current) is reduced.

3.16. Jitter by s-capacitor

The visual jitter performance can be improved by adding a damping network parallel to s-correction capacitor. This R/C/diode network is comparable to R213, C132 and D60 in our 15" Mk2 demo monitor (please refer to Application Note AN95086 circuit diagram at page 30, Fig 10).

3.17. Jitter at 24 KHz mode

At 24 KHz the jitter performance will be relative high due to the low current in TDA4855/58 HREF resistor. At this typical frequency jitter performance can be improved by changing the oscillator capacitor i.s.o. resistor value. The application circuit is connected to TDA4855/58 pin 29. Please refer to Application Note AN95087 page 19, figure 13 for the application circuit.

3.18. Jitter by DAC/PWM

The filtering of the DC control signals should be improved. Long tracks should have one filter close to the DAC/PWM and another one close to the TDA4855/58. According to experience that 3 -5 cm is about the maximum wiring that is allowed without filtering. Longer wires must be filtered.

3.19. B+ drive crosstalk

There is chance that vertical lines on the picture will show two small kinks, one in the upper half of the picture and one in the lower half. This typically occurs only in one mode, at a certain H-frequency. This phenomenon appears when there is crosstalk between the H-drive and B-drive signals where B-drive is modulated with EW parabola in TDA4855/58. At certain modes and/or picture width setting the trailing edge of B-drive coincides with the leading edge of H-drive (two times per V-period). To solve this we should:

1) Keep the copper tracks and component on the TDA4855/58 BIN and BOP pins small to prevent pick-up by the HDRV track or from the steep edges of the H-drive stage at the start of Ibase.

2) Keep the voltage swings at pins HDRV and BDRV low to prevent capacitive crosstalk between these pins and their board tracks.

3) Keep the current loading on pins HDRV and BDRV low to prevent crosstalk inside the IC by using series resistors.

3.20. jitter/Noise by vertical booster

To avoid magnetic interference the loop area between the vertical differential output of the TDA4855/58 and the differential input of the vertical booster (for instance TDA4866) should be as small as possible. The filters for the output/input should be applied as in our 15“ Mk2 monitor (please see circuit diagram in Application Note AN95086 page 29, Fig 9; the mentioned filter components are C304, C305, R301, R302, C95, C106, R154, R168). The ground of the filter components on TDA4866‘s input lines should be connected with a separate track to TDA4866 pin 5.

3.21. Waterfall noise

Our recommendation is use a low ohmic damping resistor parallel to vertical deflection yoke (total resistor value around 130 ohms including any resistor on the CRT/coil combination).

3.22. SMPS noise

Around the SMPS and EHT transformer there is a ground loop. Due to the leakage field of these transformers large currents are induced in the ground tracks. Be aware that this can cause disturbances at the screen.

3.23. Jitter by Diamontron tube

The visual jitter on the screen must have other causes, for instance the magnetic leakage field of the SMPS transformer entering the picture tube neck. This phenomenon depends on the phase relation between the displayed vertical line and the actual vertical phosphor stripe. When these are not perfectly parallel, then we can find alternating regions along the vertical line where the jitter is yes/no visible. In this case the trinitron like shadow mask of the Diamontron tube makes any remaining jitter much more visible.

3.24. Current inputs

The pins of TDA4855/58 VPOS, VAMP, VSCOR, EWTRP, EWPAR, HPOS, EWWID are current inputs. This means the voltage is independent of the input current (input current range = 0 to 120 uA, input voltage = 5 V). This input architecture is chosen for ease of adding independent input signals on one pin. Interfering radiation with E-field nature are also added. It‘s therefore recommended to keep the tracks at these pins as short as possible.

In case a long wire at these pins is inevitable an input filter is required. As the input voltages of these pins are fixed a capacitor is not effective (capacitor can only short circuit signals when there is a voltage difference across the capacitor). By means a small resistor in series with the current input pins a voltage is generated. Now a capacitive filtering can be effective. An extra series resistor might be necessary when the interference is very strong. As HPOS is not a real current inputs (has some series resistance of its own) here a direct filtering will do.

3.25. B+ converter

The LC filter (between B+ power MOSFET and FBT) will cause slow speed in changing mode. In our 15“ Mk2 monitor such a filter is not used (cost reduction and faster response on frequency changes). Due to the fact that on one end of the EHT transformer there is the normal flyback voltage and on the other end a square wave voltage so the removal of this filter has two drawbacks:

1) Temperature increase of the EHT transformer (dependent of transformer construction). With Philips transformer the temperature increase is about 4 degrees C.

2) Ringing due to MOSFET switching that has to be damped by means of a parallel LRC filter in series with EHT transformer (please see 15“ Mk2 monitor‘s circuit diagram in Application Note AN95086 page 30, Fig 10; the mentioned LRC are L9, R104 and C63).

4. REFERENCES

1. AN95086 PCALE 15“ Autosync Monitor MkII circuit description by Mr. Han Misdom
2. AN95087 Autosync Deflection controllers TDA4855 and TDA4858 by Mr. Gied Habraken
3. TDA4855 Datasheet Autosync Deflection Controller issued 1996 July 18.
4. TDA4866 Datasheet full bridge current driven vertical deflection booster issued 1995 Aug 31.
5. Emails From PS-SLE M/S Dick Teuling, Han Misdom, Hans Verhees and Hamburg CIC Mr. Paul Sonnenberger.